What is claimed is:

1. A semiconductor device comprising:

a plurality of first bump electrodes arranged on a main surface, and each of said plurality of first bump receiving signals or power;

a plurality of dummy bump electrodes arranged on said main surface, and each of said plurality of dummy bump electrically connected to associated one of said plurality of first bump electrodes.

2. The semiconductor device as claimed in claim 1 further comprising:

a plurality of protection circuit electrically coupled to said plurality of first bump electrodes.

3. The semiconductor device as claimed in claim 1, further comprising:

a plurality of test electrodes electrically connected to said first bump electrodes.

4. The semiconductor device as claimed in claim 3, wherein

said plurality of test electrodes being arranged along four edges of said semiconductor device.

5. The semiconductor device as claimed in claim 1, wherein said plurality of dummy bump electrodes being higher than said plurality of chip electrodes.

6. The semiconductor device as claimed in claim 1, wherein said

plurality of dummy bump electrodes being arranged closer than said plurality of first bump electrodes.

7. The semiconductor device as claimed in claim 1, wherein said plurality of dummy bump electrodes being arranged between said plurality of first bump electrodes and said plurality of said chip electrodes.

8. The semiconductor device as claimed in claim 1, wherein said plurality of dummy bump electrodes being provided for relaxation of stress at mounting said semiconductor device.

9. The semiconductor device as claimed in claim 1, wherein said plurality of dummy bump electrodes and said plurality of first bump electrodes being arranged alternately along to circumference of bump group.

10. A semiconductor device comprising:

a semiconductor substrate;

an insulating layer formed above said semiconductor substrate;

a plurality of first bump electrodes formed on said insulating layer, and each electrically connected to associated one of plurality elements formed in said semiconductor substrate; and

a plurality of second bump electrodes formed on said insulating layer, and each electrically connected to associated one of said plurality of first bump electrodes.

11. The semiconductor device as claimed in claim 10, further

comprising:

a plurality of test pad formed on said insulating layer, and each electrically connected to at least associated one of plurality of first bump electrodes.